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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,447	12/18/2001	Thomas D. Fletcher	2207/11269	1709

23838 7590 08/11/2006

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EXAMINER	
MAI, TAN V	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,447	FLETCHER, THOMAS D.	
	Examiner	Art Unit	
	Tan V. Mai	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39,41 and 42* is/are pending in the application.

4a) Of the above claim(s) *1-9 and 26-31* is/are withdrawn from consideration.

5)☒ Claim(s) *32-39,41 and 42* is/are allowed.

6)☒ Claim(s) *10,11,13,14,17-19 and 22-25* is/are rejected.

7)☒ Claim(s) *12,15,16,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 10, 13, 17 and 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ware (US Pat. 4,623,982).

Rejection grounds continue to be those set forth in the previous office action dated 12/15/04, paragraph 5.

3. Claims 14 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware (US Pat. 4,623,982).

Rejection grounds continue to be those set forth in the previous office action dated 12/15/04, paragraph 8.

4. Claims 11 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Ware in view of Vo et al (US Pat. 4,737,92).

Rejection grounds continue to be those set forth in the previous office action dated 12/15/04, paragraph 10.

5. Applicants' arguments filed on 5/8/06 have been fully considered but they are not persuasive.

Applicants, in his remarks, argues that:

(1). "[w]ith respect to claim 10, it Is noted that a carry generation block is to determine exactly three of the carry-out values. A carry-out value is defined earlier in the claim as being determined for each propagate value based on the propagate value and the corresponding generate value. Accordingly, three carryout values being generated by a carry generation block would require three propagate values. The current Office Action provides a marked up version of Fig. 3A from Ware. Of course, Ware describes the entire circuit of Figure 3A as a "block" with three individual cells (i.e., a start cell, a continue cell, and an end cell). In the drawing, the selective parts of the circuit are circled and denoted as a *carry generation block." Applicant respectfully disagrees. If C IN 0 (1), C IN 1 (1), and C IN (1) are to be denoted as carry-out values, then according to the claim, each carryout value would be determined for each propagate value based on the propagate value and the corresponding generate value. Looking at the circled circuit of Fig. 3A, **propagate signal P(1)** is an "input" to this denoted circuit. No other propagate signals would be inputs to this denoted circuit. Accordingly, the circuit labeled "carry generation block does not generate three carry-out values, each being determined for each propagate value as recited in claim 10. Likewise, claim 17 recites a çarry generation block that is connected to exactly three of the propagate outputs and three of the generate outputs, and the "carry generation block" has a plurality of carry outputs. As indicate above, the circuit labeled "carry generation block" has only one propagate input, not three"; and

(2) "[a]s to the rejection of claims 11 and 18 under 35 U.S.C. 103(a), Vo fails to make up for the deficiencies of Vo. In Vo, each individual bit adder 61 in Fig. 5 is to take in two bits to add and a carry in from the previous bit adder and generate a carry out for the next bit adder. There is no disclosure in Vo or Ware of a carry generation block that determines exactly six of the carry out values as described in claims 11 and 18" (emphasis added).

With respect to the arguments, the examiner carefully reviews claimed invention and the applied references.

First, the examiner believes Ware teaches the claimed invention. See the copy of Applicant's claim 10 with Ware below:

10. A method of adding two multi-bit addends, the method comprising:

receiving two multi-bit addends **[Ware's Fig. 3B; A0-8, B0-8]**;

determining a propagate value **[Ware's Fig. 3A; K(i)]** and a corresponding generate value **[Ware's Fig. 3A; G(i)]** for each bit of the addends;

determining a carry-out value **[Ware's Fig. 3A; C IN (i)]** for each propagate value **[K(i)]** based at least in part on the propagate value **[K(i)]** and corresponding generate value **[G(i)]**, wherein the carry-out values **[C IN (i)]** are determined by a plurality of carry generation blocks **[e.g., see Ware's Fig. 3B; three blocks]**, and wherein one of the carry generation blocks **[e.g., see Ware's Fig. 3B; middle block]** determines exactly three of the carry-out values **[e.g., see Ware's Fig. 3B middle block or Fig. 3A]**; and

determining a sum value **[e.g., see Ware's Fig. 3A; SUM (1) output of EX-OR gate (40)]** for each carry-out value based at least on part on the carry-out value.

It is noted that Applicant's Propagate value P(i) is the same as Ware's Propagate value K(i), e.g., see Ware, col. 1, lines 44-53. Also, it is noted that Applicant's Propagate value P(i) and Ware's Propagate value K(i) are the outputs of **OR gates**.

Second, **(1)** Vo et al disclose, e.g., see Fig. 5, a plurality of variable block adders, i.e., the sizes are two to six bit and **(2)** Ware discloses, e.g., see Figs. 3-4, a

plurality of variable block adders, i.e., the sizes are two to four bit. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Vo in Ware, thereby making the claimed invention, because the proposed device is a carry look-ahead adder having different block sizes as claimed.

Therefore, the rejections are still proper.

6. Claims 12, 15-16, and 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: the recorded references do NOT teach or suggest the amended features as recited in independent claims 32 and 37.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (571) 272-3726. The examiner can normally be reached on Mon-Wed and Fri. from 9:30am to 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is:

Official (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Tan V. Mai
Primary Examiner

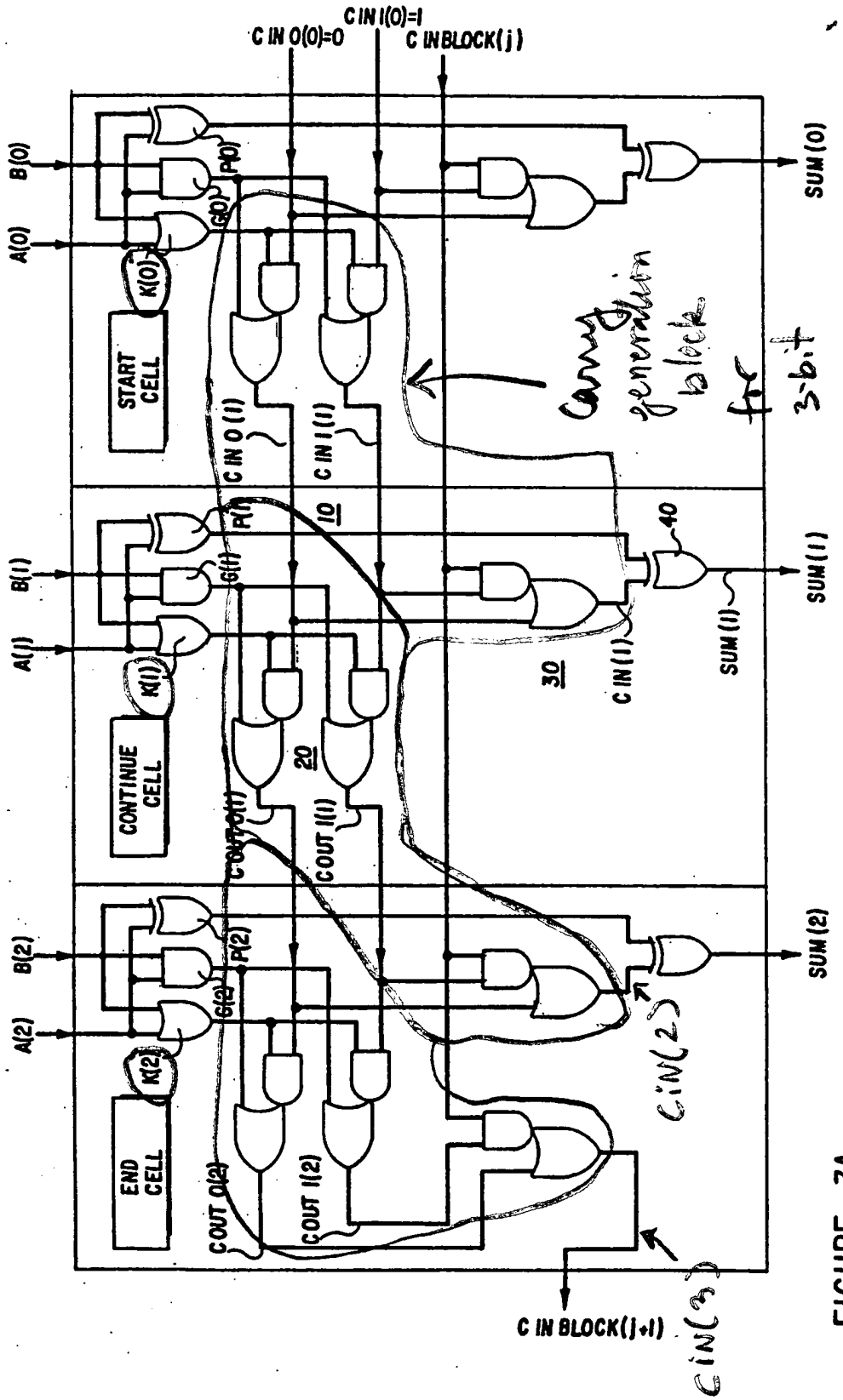
C IN O(0)=0
C IN I(0)=1
C IN BLOCK(j)
B(0)
A(0)
P(0)
G(0)
K(0)
START CELL
C IN O(1)
C IN I(1)
SUM(0)
carry generation block for 3-bit
10
40
B(1)
A(1)
P(1)
G(1)
K(1)
CONTINUE CELL
20
30
C IN(1)
SUM(1)
C OUT O(1)
C OUT I(1)
B(2)
A(2)
P(2)
G(2)
K(2)
END CELL
SUM(2)
C IN(2)
C OUT O(2)
C OUT I(2)
C IN BLOCK(j+1)
C IN(3)

FIGURE 3A